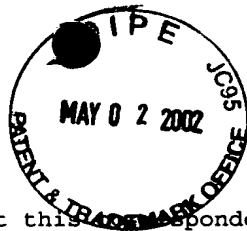


GR 98 P 2544 P



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By: Loren D. Pearson

Date: 4/24/02

#9/Amendment
Andino
5/16/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Horst Belau et al.
Appl. No. : 09/804,323
Filed : March 12, 2001
Title : Printed Circuit Board Configuration with a
Multipole Plug-In Connector
Examiner : Kamand Cuneo
Group Art Unit : 2827

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A M E N D M E N T

Hon. Commissioner of Patents and Trademarks
Washington, DC 20231

S i r :

Responsive to the Office action dated January 31, 2002, kindly
amend the above-identified application as follows:

In the Specification:

At page 9, line 18, insert the following paragraph:

--Fig. 3 is a sectional view of a printed circuit board having
two outer board layers.--

After page 12, line 17, insert the following paragraph:

--Fig. 3 shows a printed circuit board configuration. The configuration includes a first outer board layer 3, an inner board layer 10', and a second outer board layer 3' remote from the first outer board layer 3. The first outer board 3 and the second outer board layer 3' each define a respective outer edge region. As in the embodiment shown in Fig. 1, the configuration includes a first plurality of signal conductor tracks 4.1, 4.2, and 4.3, a first plurality of plug pins 8.1, 8.2, and 8.3, and a first plurality of ground conductor tracks 6.1, 6.2, and 6.3, all being disposed in a first side-to-side configuration. In addition, a second plurality of signal conductor tracks 4.1', 4.2', and 4.3' are disposed in the edge region of the second outer board layer. The configuration also includes a second plurality of plug pins 8.1', 8.2', and 8.3'. Each one of the second plurality of the plug pins 8.1', 8.2', and 8.3' is fixed to a respective one of the second plurality of the signal conductor tracks in a direction parallel to the second outer board layer 3'. A second plurality of ground conductor tracks 6.1', 6.2', 6.3', and 6.4' are disposed on the second outer board layer 3' and are assigned to the second plurality of the signal conductor tracks 4.1', 4.2', and 4.3'. All of these second signal conductor tracks 4.1', 4.2', and 4.3', plug pins 8.1', 8.2', and 8.3', and ground conductor tracks 6.1', 6.2', 6.3', and

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6.4' are disposed in a second side-to-side configuration in which the second plurality of the signal conductor tracks 4.1', 4.2', and 4.3' and said the plurality of the ground conductor tracks 6.1', 6.2', 6.3', and 6.4' are alternately disposed on the second outer board layer 3', and in which the second plurality of the signal conductor tracks 4.1', 4.2', and 4.3' run essentially parallel with respect to the second plurality of the ground conductor tracks 6.1', 6.2', 6.3', and 6.4'.--

Remarks:

Reconsideration of the application is requested. Claims 1-7 remain in the application.

In item 1 of the Office action, the Examiner refused to grant priority for the reason that the priority application was not specified in the declaration. The Examiner is directed to the second full paragraph on page 1 of the declaration, which reads: "German Application No. 198 41 459.5, filed September 10, 1998, the International Priority of which is claimed under 35 U.S.C. §119." Section 119(b)(1) states the following:

No application for patent shall be entitled to this right of priority unless a claim is filed in the Patent and Trademark Office, identifying the foreign application by specifying the application number on that foreign application, the intellectual property authority or country in or for which the application was filed, and the date of filing the application.

In this case, a claim was made in the declaration. The foreign application was identified by its application number, DE 198 41 495.5. The intellectual property authority was "German". The filing date was listed as "September 10, 1998". Accordingly, the requirements for 35 U.S.C. § 119 were met by the declaration.

In item 2 of the Office action, the Examiner incorrectly required a copy of the parent international application. Priority of the PCT application has been claimed under 35

U.S.C. § 120; *see also* MPEP § 1895. Section 120 states the following:

An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, as though filed on the date of the prior application, if filed before the patenting or abandonment of or termination of proceedings on the first application or on an application similarly entitled to the benefit of the filing date of the first application and if it contains ... a specific reference to the earlier filed application.

In this case, the instant application was filed on March 12, 2001. The parent application was filed on September 2, 1999, and claimed a priority date of September 10, 1998. The thirty-month duration of the international application ended on March 10, 1998, which was extended to March 12, 2001, because March 10, 1998, was a Saturday. Enclosed find PCT forms 416 and 409, which are from the Preliminary Examination and show that the international application was pending for 30 months from the priority. The specification, page 1, lines 7-9, cross-references the parent application. Therefore, by being copending and cross-referencing the parent application, all of the requirements to claims priority under 35 U.S.C. § 120 have been met. Furthermore, because 35 U.S.C. § 120 does not require that a copy of the international application be forwarded, none is included herewith.

In item 4 of the Office action, the Examiner objected to the drawings because they did not show every feature of the claims. More specifically, the Examiner objected that the drawing did not show the feature of claim 7: namely, the second outer layer with the conductors, ground tracks, and pins. Fig. 3 has been added. In addition, a brief description of Fig. 3 has been added as well as a final paragraph to the specification. The final paragraph tracks the language of claim 7 and therefore adds no new matter. Furthermore, because Fig. 3 is substantially a double image of the configuration shown in Fig. 1 that was described in the original specification in claim 7, the addition of Fig. 3 introduces no new matter.

The changes to the specification are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In item 7 of the Office action, the Examiner rejected claims 1-6 as being obvious over Gentry (U.S. 4,644,092), Osifchin et al. (U.S. 3,093,805), and Kobayashi et al. (U.S. 6,040,524) under 35 U.S.C. § 103(a). As will be explained below, the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, a brief review of the invention as claimed is provided. Claim 1 calls for, *inter alia*, a printed circuit board configuration with a multipole plug-in connector having the following features:

a board having at least two layers, each one of said at least two layers having an edge region;

a plurality of signal conductor tracks disposed in said edge region of one of said layers;

a plurality of plug pins, each one of said plurality of said plug pins fixed to a respective one of said plurality of said signal conductor tracks in a direction parallel to said one of said layers;

a plurality of ground conductor tracks disposed on said one of said layers and assigned to said plurality of said signal conductor tracks;

a side-to-side configuration in which said plurality of said signal conductor tracks and said plurality of said ground conductor tracks are alternately disposed on said one of said layers, and in which said plurality of said signal conductor tracks run essentially parallel with respect to said plurality of said ground conductor tracks;

at least one filter capacitor connected between a respective one of said plurality of said signal conductor tracks and a respective one of said plurality of said ground conductor tracks; and

a ground shielding surface disposed on an adjacent one of said layers and covering said side-to-side configuration.

Gentry does not teach or suggest the details of the connection between the contact members and the conductors. Gentry does teach that a cable 12 has a plurality of conductors 16 that are disposed between the inner surfaces of a first insulating

substrate 18 and second insulating substrate 22; see col. 2., ll 33-34. Also in Gentry, a graphically formed shield 14 is applied onto the outer surface 24 of the second insulating substrate 22. In the edge region of the substrates 18 and 22, contact members 26 are connected with the conductors 16; see Fig. 5 and col. 2, ll 61-62. Furthermore, in all of the figures of Gentry, the region in which the contact members 26 are connected with the conductors 16 are not covered with the conducting shield, but rather are completely open.

In contrast to Gentry, in the invention of the instant application as claimed, ground conductor tracks run between the signal conductor tracks (as recognized by the Examiner) and the side-by-side configuration of signal and ground conductor tracks should be on one board layer. In addition, the invention claims that a ground shielding surface covering the surface region of the signal and the ground conductor tracks should be on a neighboring board layer: i.e. the opposite board layer in a two-layer configuration.

The ground shielding surface is thus in the region of the connection of the signal conductor tracks and the plug pins, and not, as in Gentry, in an adjacent area.

In addition, the subject matter of the instant application pertains to printed circuit board configurations with a board and not to a flexible substrate, such as a flexible cable.

Therefore, especially when aggregated, the invention of the instant application claims significantly different features than those taught by Gentry. For the reasons detailed below, Kobayashi and Osifchin do not teach or suggest these features.

Kobayashi as well as Osifchin show printed circuit board configurations, which, in their cross section, correspond to the cross-sectional view of Fig. 2. However, no plug pins are provided therein. Furthermore, Kobayashi and Osifchin relate to high-frequency printed circuit board configurations.

Therefore, even if one with ordinary skill in the art were to be motivated by Kobayashi or Osifchin to provide, for the flexible cable of Gentry, ground conductor tracks between the conductors 16, not all of the features of the claimed invention would be taught or suggested. Specifically, no ground surface is provided in the edge region of the substrates 18 and 22. Furthermore, the ground and signal conductor tracks would still be disposed between the substrates 18 and 22 and not on an outer layer of the board. Furthermore, the subject matter that would result from a

combination of the references would still be a flexible cable and not a printed circuit board configuration.

Accordingly, none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Therefore, claim 1 is patentable over the art. Moreover, because all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-7 are solicited. In the event the Examiner should still find any of the claims to be unpatentable, please telephone counsel so that patentable language can be substituted.

Please charge any fees that might be due with respect to
Sections 1.16 and 1.17 to the Deposit Account of Lerner and
Greenberg, P.A., No. 12-1099.

Respectfully submitted,



For Applicants

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LDP:cgm

April 18, 2002

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